

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

Patent No ..... 7,057,257 B2  
Patent Issue Date ..... June 6, 2006  
Application Serial No. .... 10/071,453  
Filing Date ..... February 8, 2002  
Assignee ..... Micron Technology, Inc.  
Inventorship ..... Luan C. Tran  
Attorney's Docket No. .... MI22-1921  
Title: Plurality of Transistors Having Different Active Area Widths and Different Threshold  
Voltages Defined by STI

**REQUEST FOR CERTIFICATE OF CORRECTION OF PATENT FOR  
APPLICANT MISTAKE and PTO MISTAKES (37 C.F.R. §§ 1.322(a) and 1.323)**

To: Commissioner for Patents  
P.O. Box 1450  
Alexandria, VA 22313-1450  
ATTN: Decision and Certificate of Correction  
Branch of the Patent Issue Division  
  
From: D. Brent Kenady (Tel. 509-624-4276; Fax 509-838-3424)  
Wells St. John P.S.  
601 W. First Avenue, Suite 1300  
Spokane, WA 99201-3828

Sir:

It is hereby requested that a Certificate of Correction be issued with respect to Patent No. 7,057,257 B2, granted June 6, 2006, in accordance with the Certificate of Correction form attached hereto.

It is noted that an error appears in this patent of a typographical nature of character, as more fully described below. The error occurred in good faith. Correction thereof does not involve such changes in the patent as would constitute new matter or would require re-examination.

Other errors listed on the Certificate of Correction form were apparently incurred through the fault of the PTO as will be disclosed by the records of files in the Office.

Attached hereto, is Form PTO-1050, being suitable for printing.

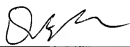
The exact page and line number where the error occurs in the application file are:

Reference AD on the Form PTO-1449 filed April 1, 2004.

The Director is hereby authorized to charge the \$100.00 fee as required under 37 CFR 1.20(a), or credit any overpayment, to Deposit Account No. 23-0925.

Respectfully submitted,

Dated: 6-8-07

By:   
D. Brent Kenady  
Reg. No. 40,045

UNITED STATES PATENT AND TRADEMARK OFFICE

**CERTIFICATE OF CORRECTION**

PATENT NO. : 7,057,257 B2

DATED : June 6, 2006

INVENTOR(S) : Tran

It is certified that errors appear in the above-identified patent and that said Letters Patent is hereby corrected as shown below:

Title Page, please delete the following title, "**SEMICONDUCTOR PROCESSING METHODS OF FORMING TRANSISTORS, SEMICONDUCTOR PROCESSING METHODS OF FORMING DYNAMIC RANDOM ACCESS MEMORY CIRCUITRY, AND RELATED INTEGRATED CIRCUITRY**" and insert -- **PLURALITY OF TRANSISTORS HAVING DIFFERENT ACTIVE AREA WIDTHS AND DIFFERENT THRESHOLD VOLTAGES DEFINED BY STI**--.

Title page 2, U.S. PATENT DOCUMENTS, please insert --6,107,134 \* 8/2000 Lu et al.-- before "6,121,651".

Title page 2, U.S. PATENT DOCUMENTS, second column, please insert --6,297,082 \* 10/2001 Lin et al.-- before "6,121,651".

Title page 2, U.S. PATENT DOCUMENTS, second column, please delete "2002/0020106" after "Berry et al. ....257/397" and insert --2003/0020106--.

Col. 1, line 63, please delete "is" after "access".

Col. 4, line 66, please delete " $V_{t1}$ ," before "while" and inert -- $V_{ti}$ --.

Col. 5, line 6, please delete " $V_{t1}$ ," after "voltage" and inert -- $V_{ti}$ --.

Col. 5, line 21, please delete "CSAL" after "signal" and insert -- $C_{SAL}$ --.

Col. 5, line 42, please delete "ca" after "tion" and insert --can--.

Col. 6, line 32, claim 6, please delete " $V_{t1}$ ," after "voltage" and inert -- $V_{ti}$ --.

Page  
1 of 1

**Mailing Address of Sender:**

D. Brent Kenady  
Wells St. John P.S.  
601 West First Avenue, Suite 1300  
Spokane, WA 99201-3828

Patent No. 7,057,257 B2